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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,526	11/25/2003	Hokyun Ahn	2013P134	8657
8791	7590	10/06/2004	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD SEVENTH FLOOR LOS ANGELES, CA 90025-1030			VU, HUNG K	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/723,526

**Applicant(s)**

AHN ET AL.

**Examiner**

Hung Vu

**Art Unit**

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 25 August 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) 6-12 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>11/25/03, 01/09/04</u> .  | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election of Invention of Group I, Claims 1-5, in the reply filed on 08/25/04 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Applicant's election without traverse of Invention of Group I, Claims 1-5, in the reply filed on 08/25/04 is acknowledged.

Claims 6-12 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Invention, there being no allowable generic or linking claim.

Election was made **without** traverse in the reply filed on 08/25/04.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fanning et al. (GaAs Mantech Conference Article, of record) in view of Tavrow et al. (PN 5,034,608).

Fanning et al. discloses, as shown in Figures 1 and 2, a semiconductor substrate comprising:

a semiconductor substrate;

source and drain electrodes, which are formed on the semiconductor substrate to make ohmic contact with the semiconductor substrate;

a T-shaped gate electrode, which is formed between the source and drain electrodes on the semiconductor substrate; and

an insulating layer (a layer of dielectric) being interposed between the gate electrode and the source and drain electrodes.

Fanning et al. does not disclose the insulating layer including a silica aerogel layer. However, Tavrow et al. discloses an insulating layer (220) being interposed between a gate electrode (206) and a source or a drain electrode (222). Note Figure 3 of Tavrow et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the insulating layer of Fanning et al. including a silica aerogel layer, such as taught by Tavrow et al. in order to reduce the noise or the coupling capacitance between the gate electrode and the source and drain electrodes.

With regard to claim 2, Fanning et al. and Tavrow et al. disclose the insulating layer is formed of a composite layer of the silicon nitride layer and the silica aerogel layer.

With regard to claims 3-5, Fanning et al. and Tavrow et al. disclose the silicon nitride layer has a thickness of 1000 Å (within a range of 100-1000Å). Fanning et al. and Tavrow et al. do not disclose the silica aerogel layer has a thickness greater than the thickness of the silicon nitride layer or the thickness of the aerogel layer. Although Fanning et al. and Tavrow et al. do not teach the thickness of the aerogel layer, as that claimed by Applicant, however, it would have

Art Unit: 2811

been obvious to one having ordinary skill in the art at the time the invention was made to form the aerogel layer having a desired thickness, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moon et al. (P1997-0018657, of record) in view of Tavrow et al. (PN 5,034,608).

Moon et al. discloses, as shown in Figure (E), a semiconductor substrate comprising:

- a semiconductor substrate (11);

- source and drain electrodes (15,17), which are formed on the semiconductor substrate to make ohmic contact with the semiconductor substrate;

- a T-shaped gate electrode (21), which is formed between the source and drain electrodes on the semiconductor substrate; and

- an insulating layer (13) being interposed between the gate electrode and the source and drain electrodes.

Moon et al. does not disclose the insulating layer including a silica aerogel layer. However, Tavrow et al. discloses an insulating layer (220) being interposed between a gate electrode (206) and a source or a drain electrode (222). Note Figure 3 of Tavrow et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the insulating layer of Moon et al. including a silica aerogel layer, such as taught by Tavrow et al. in order to reduce the noise or the coupling capacitance between the gate electrode and the source and drain electrodes.

Art Unit: 2811

***Conclusion***

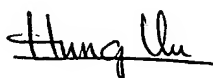
4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The Central Fax Number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

September 24, 2004

A handwritten signature in black ink, appearing to read "Hung Vu", written over a horizontal line.

Hung Vu

Patent Examiner